REMARKS

Claims 1 to 23 are pending in the application. Claims 1, 7, 10 and 17 are independent. Favorable reconsideration and further examination are respectfully requested.

Initially, Applicants noted that the cover sheet of the Office Action indicates that only claims 10 to 23 are pending, with remaining claims 1 to 9 having been withdrawn from consideration due to an earlier restriction requirement. However, the body of the Office Action includes rejections of claims 1 to 9, in addition to rejections of claims 10 to 23.

In view of the foregoing discrepancy, the undersigned telephoned the Examiner on January 15, 2003 to request clarification. During that telephone conversation, the Examiner indicated that the restriction should be ignored and that the response should address all of the rejected claims, including claims 1 to 9. Applicants are proceeding accordingly.

Claims 1 to 4, 7 and 9 were rejected under 35 U.S.C §102(b) over U.S. Patent Application Publication 2002/0043686 (Bolam); claims 5, 6, 8, 10 to 15 and 17 to 22 were rejected under §103 over Bolam; and claims 16 and 23 were rejected under §103 over U.S. Patent No. 6,251,782 (Lee). As shown above, Applicants have amended the claims to define the invention with greater clarity. In view of these amendments, reconsideration and withdrawal of the art rejections are respectfully requested.

Amended independent claim 1 is directed to a tiedown structure that includes a semiconductor substrate having a chip formed thereon, a kerf region proximate the chip, and a conductive connector forming an electrical connection between the chip and the kerf region.

Bolam is not understood to disclose or to suggest the foregoing features of claim 1, particularly with respect to "a conductive connector forming an electrically conductive connector that connects the device and the kerf".

In this regard, it was said in the Office Action that Fig. 7A of Bolam discloses a conductive connector 202 which forms a connection between the chip and the kerf regions. Paragraphs 0051 and 0052 were cited in support of this proposition. Applicants respectfully disagree with this characterization of Bolam. As understood by Applicants, Bolam's diffusion protect layer 202 does not form an electrical connection, but rather is used as a diffusion barrier to protect oxide layer 212 from impurities. Furthermore, Bolam's diffusion protect layer 202 does provide a connection between the chip and the kerf region 206 (i.e., "where a dicing saw will cute the SOI chips apart along line 208" - paragraph 0052). As shown in Fig. 7A, diffusion protect layer 202 does not even reach the kerf region 208.

For at least the foregoing reasons, Applicants submit that claim 1 is different from, and therefore patentable over, Bolam.

Amended independent claim 7 defines a tiedown structure that includes a semiconductor substrate having a chip formed thereon, an edge seal along an outer perimeter of the chip, and a conductive connector forming an electrical connection between the edge seal and a portion of the chip. Bolam is not understood to disclose or to suggest these features.

More specifically, as noted above, diffusion protect layer 202 (Fig. 7A of Bolam) does not provide an electrical connection, nor does it connect an edge seal on an outer perimeter of a chip and a portion of the chip. In fact, there is no mention in the cited portion of Bolam of an edge seal. Accordingly, claim 7 is believed to be patentable.

Amended independent claim 10 is directed to a method for forming a semiconductor structure that includes forming a device on a chip, defining a kerf close to the chip, and forming an electrically conductive connector that connects the device and the kerf.

The applied art is not understood to disclose or to suggest the foregoing features of claim 10. In particular, Bolam is not understood to disclose or to suggest forming an electrically conductive connector that connects the device and the kerf. As explained above, diffusion protect layer 202 does not form an electrical connection, nor does it connect the device and the kerf. Accordingly, claim 10 is believed to be allowable.

Amended independent claim 17 defines a method for forming a tiedown structure, which includes forming a chip on a semiconductor substrate, the chip including a device, forming an edge seal along an outer perimeter of the chip, and forming an electrically conductive connector. The conductive connector connects the edge seal and the device.

As explained above, diffusion protect layer 202, which was said in the Office Action to correspond to electrically conductive conductor, does not provide an electrical connection or connect an edge seal to the device. Accordingly, claim 17 is believed to be allowable.

In view of the foregoing amendments and remarks, the entire application is believed to be in condition for allowance and such action is respectfully requested at the Examiner's earliest convenience.

All correspondence should be directed to the undersigned at the address shown below. Applicants' undersigned attorney can be reached by telephone at the number shown below.

No fee is believed to be due for this Amendment, since this Amendment is being filed within the three-month statutory period, taking into account the Presidents' Day Holiday on

February 17, 2003 and the closure of the Patent Office on February 18, 2003 due to the Presidents' Day snowstorm. However, if any fees are due for this Amendment, please apply such fees to Deposit Account No. 06-1050 referencing Attorney Docket 13292-009001.

Respectfully submitted,

Date: February 19, 2003

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

--1. (Amended) A tiedown structure, comprising:

a semiconductor substrate having a chip formed thereon;

a kerf region proximate the chip; and

a conductive connector forming [a] an electrical connection between the chip and the kerf region.

7. (Amended) A tiedown structure comprising:

a semiconductor substrate having a chip formed thereon;

an edge seal along an outer perimeter of the chip; and

a conductive connector forming [a] an electrical connection between the edge seal and a portion of the chip.

10. (Amended) A method for forming a tiedown [semiconductor] structure, comprising:

forming a device on a chip;

defining a kerf proximate the chip; and

forming [a] an electrically conductive connector, the conductive connector connecting the device and the kerf.

17. (Amended) A method for forming a tiedown [semiconductor] structure, comprising:

forming a chip on a semiconductor substrate, the chip including a device;

forming an edge seal along an outer perimeter of the chip; and

forming [a] an electrically conductive connector, the conductive connector connecting the edge seal and the device.--